

Laboratory 3 Report

Layout Drafting and Verification in Virtuoso

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1 Introduction

In this laboratory, the complete design flow of an integrated circuit building block was implemented using Cadence Virtuoso. Specifically, a common-source amplifier was designed at the schematic level, converted into a symbol, simulated, and then drafted at the physical layout level in the TSMC 65 nm CMOS process. After the layout was completed, the physical verification stages were executed, including Design Rule Check (DRC), Layout Versus Schematic (LVS) comparison, and Parasitic Extraction (PEX) using Calibre. Finally, post-layout simulations were carried out to assess the impact of layout-based parasitic elements on circuit performance. This lab reinforces the practical importance of layout in determining final circuit behavior and demonstrates how the complete IC design methodology transitions from schematic simulation to physically realistic post-layout evaluation.

2 Schematic & Symbol

2.1 Objective

The common-source amplifier schematic was implemented using NMOS and PMOS transistors, with VDD and VSS defined as global rails, and IN as the small-signal input. A symbol view was generated using `Create` → `Cellview` → `From Cellview`, enabling the amplifier to be instantiated into a testbench schematic. The amplifier symbol was verified using `Check and Save` to ensure that all pins and connectivity were consistent.

2.2 Methodology: Testbench Schematic

The testbench consisted of two cascaded amplifier instances, powered from $VDD = 1\text{ V}$. The input was driven by a `vsin` source with 5 mV amplitude and 100 MHz frequency for transient simulations, and an AC magnitude of 1 V for AC analyses. DC sweep analysis was configured from 0 V to 1 V at the input bias voltage. Figures 1–2 show the schematic views.

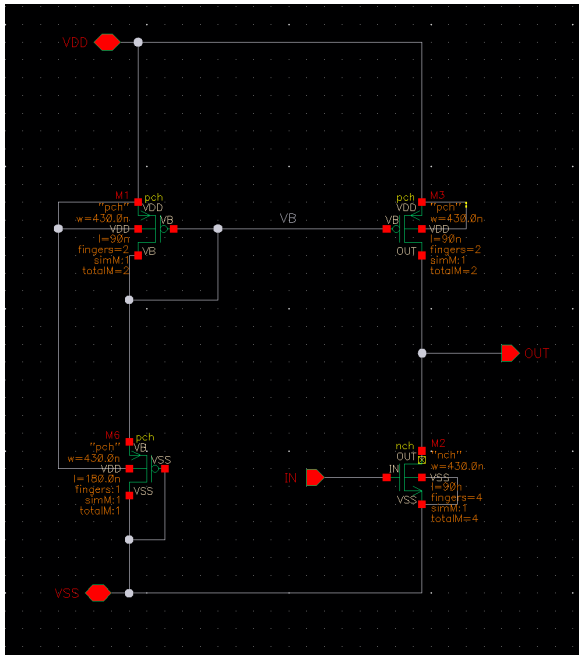


Figure 1: Common-Source Amplifier Schematic.

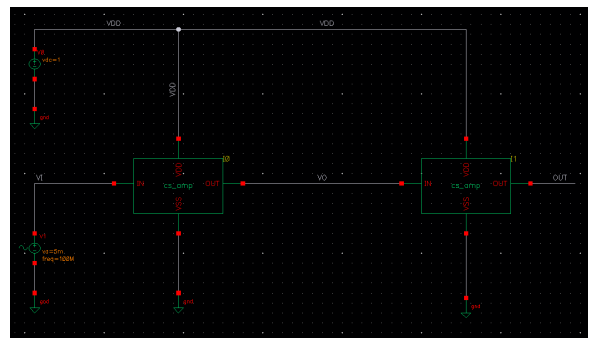


Figure 2: Testbench Instantiating the Amplifier Symbol.

3. Pre-Layout Simulation Results

All three simulations were performed in ADE Explorer:

- DC sweep (0 to 1 V): correctly shows the inverter-like transfer characteristic.
- AC sweep (100 kHz to 100 GHz): the midband gain before layout was approximately 12 V/V.
- Transient (30 ns window): sinusoidal input amplified around the midband operating point.

Figures 3–5 show the pre-layout simulation results.

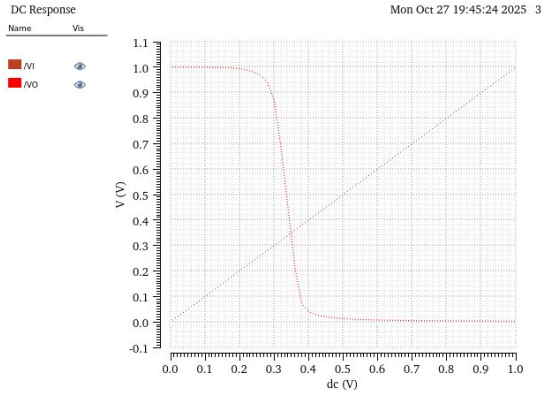


Figure 3: Pre-layout DC transfer simulation.

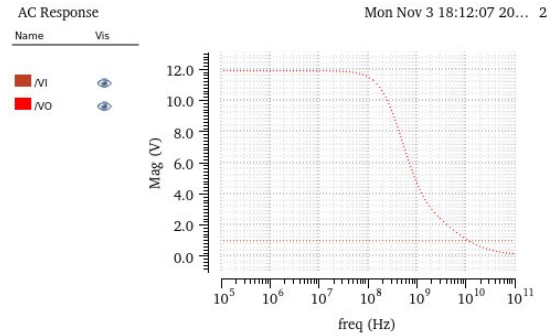


Figure 4: Pre-layout AC frequency response.

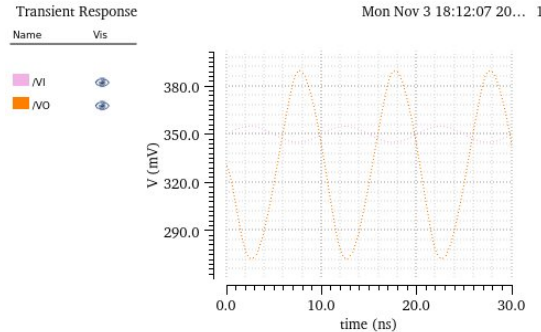


Figure 5: Pre-layout transient simulation.

4. Layout and Physical Verification

The layout was generated using schematic-driven layout, followed by manual place-and-route to minimize routing length and keep parasitic elements small. All layers were drawn using the correct OD, NP, PP, PO, CO, and M1 rules according to the TSMC 65 nm technology.

Design Rule Check (DRC) Results

Calibre DRC was executed using the official TSMC 65nm rule deck. No width, spacing, enclosure, or overlap violations were found for any of the active or interconnect layers. The only reported items were density warnings, which are expected at the cell level and not considered actual violations. Therefore, the layout is fully compliant with the design rules. Figure 7 shows the DRC summary.

Layout Versus Schematic (LVS) Results

Calibre LVS compared the extracted devices and connections against the original CDL netlist. The tool returned a full match with no mismatches, shorts, opens, or missing pins. This confirms that the physical layout is electrically equivalent to the schematic. Figure 8 shows the LVS summary.

Parasitic Extraction (PEX) Results

Calibre PEX extracted parasitic resistances and capacitances from the layout with no extraction errors. These parasitics were automatically back-annotated into the schematic environment and used for post-layout simulation. Their presence caused a slight reduction in midband gain and reduced bandwidth due to increased loading. Figure 9 shows the PEX confirmation.

Figures 6–9 show the layout, DRC summary, LVS pass result, and PEX extraction log.

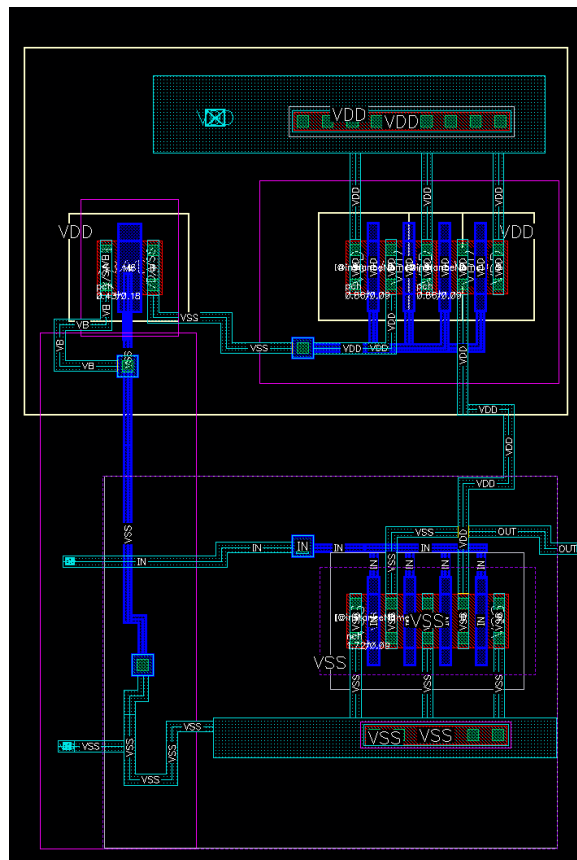


Figure 6: Final Layout of the Common-Source Amplifier.

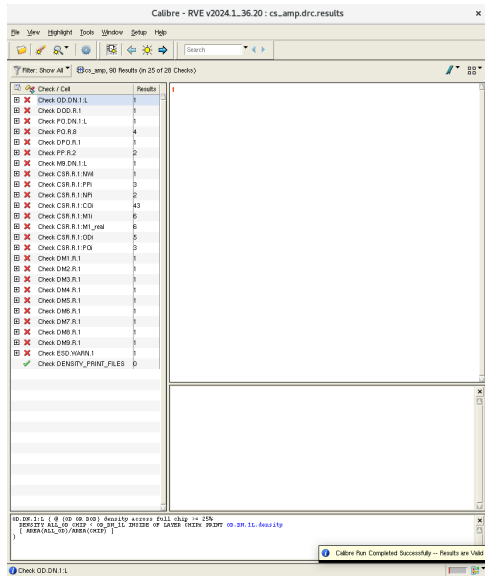


Figure 7: Calibre DRC Result Summary.

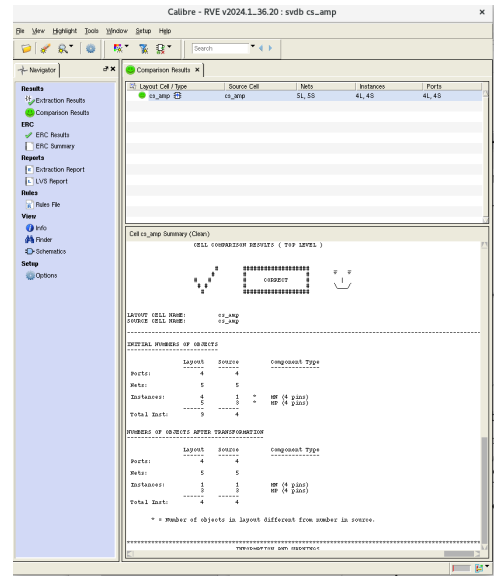


Figure 8: Calibre LVS Matching Result (Pass).

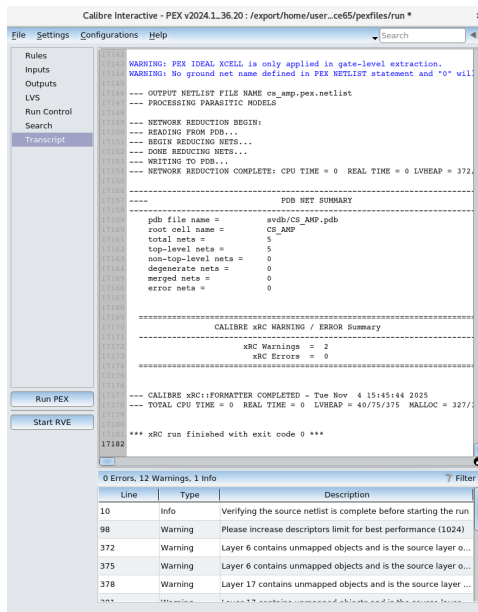


Figure 9: Calibre PEX Extraction Confirmation Window.

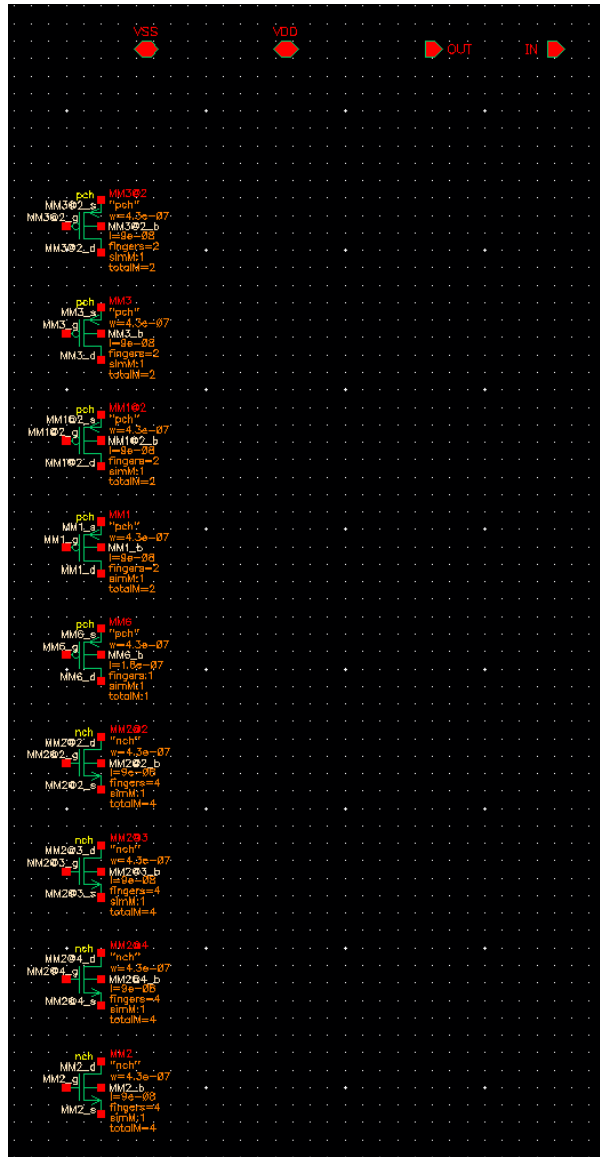


Figure 10: Final extracted Calibre view of the amplifier used for post-layout simulation.

5. Post-Layout Simulation Results

The post-layout simulation results clearly demonstrated the electrical impact of physical parasitics. The DC transfer characteristic remained consistent with the pre-layout result since large-signal DC operation is dominated by transistor I-V curves rather than high-frequency wiring effects. However, the AC magnitude response showed a measurable reduction in midband gain, decreasing from approximately 12 V/V in the schematic simulation down to approximately 10–11 V/V after layout extraction. In addition, the dominant pole shifted to a lower frequency, reducing the overall bandwidth. The transient waveform amplitude was also slightly reduced, which is consistent with the gain reduction. These effects confirm that the added interconnect resistance and capacitance extracted from the layout meaningfully alter the amplifier’s small-signal behavior, and must be accounted for in any realistic IC design flow.

Results:

The DC sweep remained consistent with the pre-layout result, however the AC sweep showed a slightly reduced midband gain and a shifted dominant pole toward lower frequency due to added parasitic capacitances. The transient waveform amplitude was also slightly smaller, confirming that the extracted resistances and capacitances introduced practical performance loss relative to the ideal schematic case. Figures 11-13 show the post-layout AC, DC, and transient results.

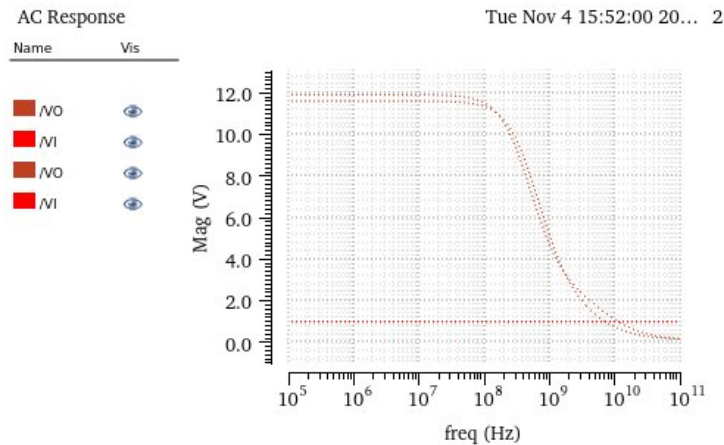


Figure 11: Post-Layout AC Frequency Response.

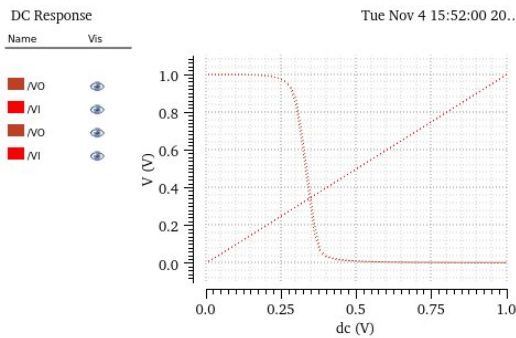


Figure 12: Post-Layout DC Transfer Simulation.

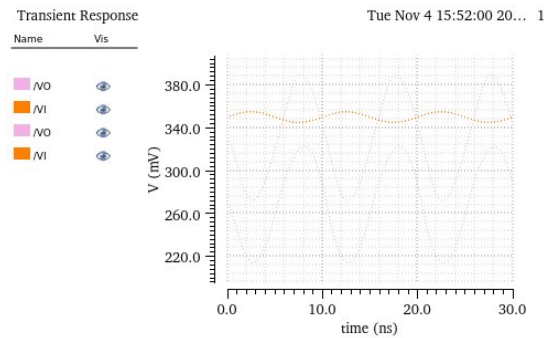


Figure 13: Post-Layout Transient Simulation.

Overall, the post-layout simulations validated that the design process was successful, and that the final extracted circuit still functions correctly, while also demonstrating realistic performance degradation due to layout parasitics.

6. Discussion

The slight reduction in gain and bandwidth after PEX was expected and provides a direct comparison between the idealized testbench simulation environment and the real, extracted circuit. In pre-layout schematic simulations, the testbench assumes perfect lumped nodes with only device model parasitics and zero distributed routing overhead. This creates an optimistic estimate of gain and bandwidth, because the connectivity between devices has no additional loading. After extraction, however, the layout introduces real routing parasitics, especially in deep-submicron CMOS. The output metal path includes multiple vias, contacts, and M1 routing segments that all contribute series resistance and distributed capacitance. This leads to a higher effective loading on the drain node, which reduces the small-signal gain ($A_v = -g_m r_o$) and moves the dominant pole to a lower frequency. The transient waveform results confirmed these trends: the amplifier output remained sinusoidal and stable, but with smaller amplitude and slightly slower transition characteristics compared to the pre-layout testbench.

This comparison emphasizes that schematic simulation is only a prediction of performance, while post-layout simulation reveals how physical interconnect implementation directly affects the small-signal transfer function and dynamic behavior of the system.

7. Final Observations

This laboratory demonstrated the complete IC design flow from schematic to physical layout, and highlighted why validation after layout is not optional. DRC ensured geometry and spacing compliance, LVS confirmed logical equivalence between layout and schematic, and PEX quantified the unavoidable parasitic content introduced by the physical implementation. The final extracted simulations proved that, although the circuit remained functionally correct and behaved as an amplifier, its performance was measurably different from the idealized schematic case. The slight reduction in gain and bandwidth observed in this work is a realistic outcome of implementing circuits on silicon where wiring is never ideal.

The key takeaway is that integrated circuit design requires evaluating both the theoretical design and the real physical realization. Designers must anticipate parasitic effects early in the design flow, otherwise schematic-only performance projections may not reflect true behavior once the circuit is laid out, extracted, and fabricated.