Laboratory 3 Report

ENGG*3450 Electronic Devices

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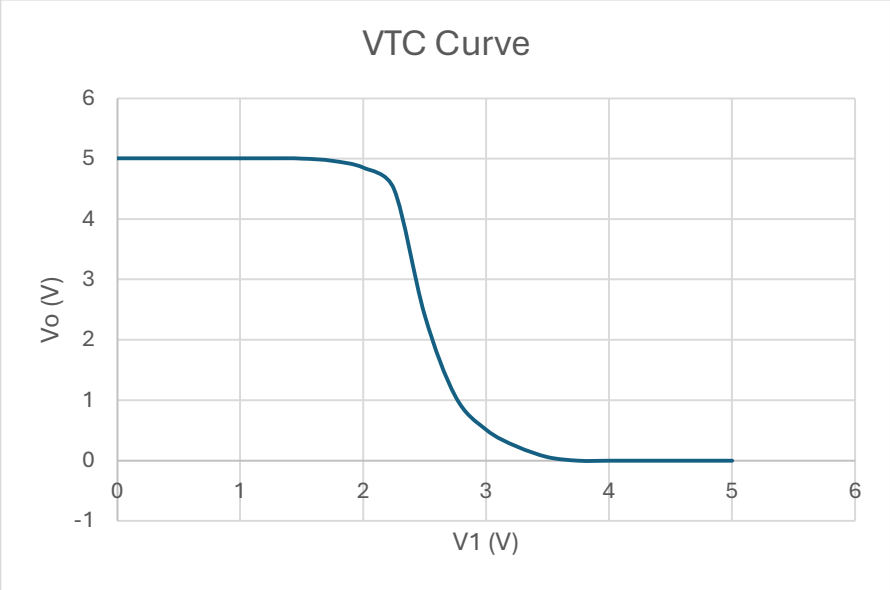
Experiment 1: VTC and Propagation Delay

Introduction

The Voltage-Transfer Characteristic (VTC) and Propagation Delay are key properties used to analyze the behaviour of digital circuits such as CMOS inverters. The VTC describes how the output voltage (V_O) of the inverter responds to changes in the input voltage (V_I). It defines the operating regions of the inverter to check the validity of logic levels (logic 0 and logic 1) and the transition region where the inverter switches states.

The propagation delay measure how quickly the inverter responds to a change in input. It is defined as the average time taken for the output to switch during a rising or falling input signal. This delay is critical for understanding the speed and timing performance of digital systems. By comparing the VTC curve and propagation delay, we can determine important parameters such as the switching threshold, noise margins, and the overall performance of the inverter. These metrics are essential for designing reliable and efficient digital circuits.

Observations



Analysis

The switching threshold at which vo = vi would be found in the middle of the slope where vo drops from 5 to 0V. It is approximately at the half way point, 2.5V.

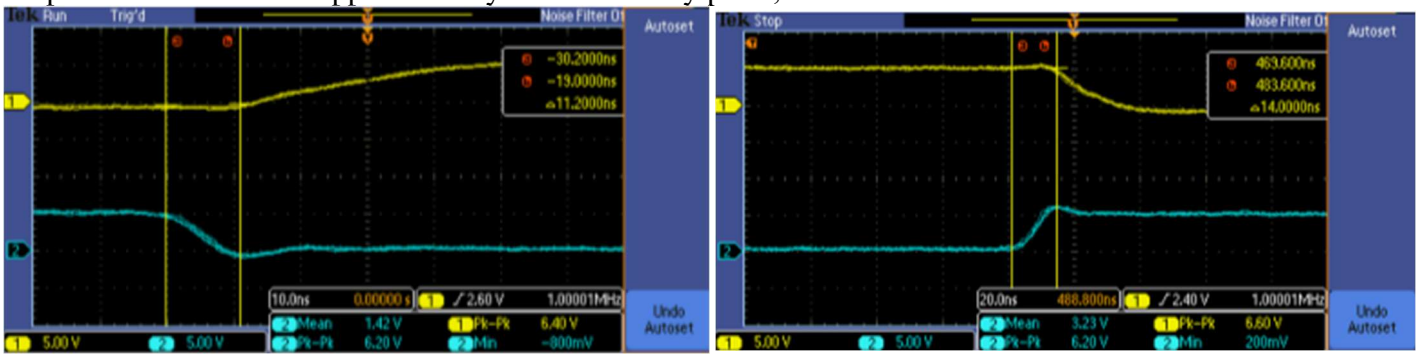


Figure 1: *The image on the left is the tphl and the image on the right is the tplh.*

From the CD4007 Datasheet, VOL = 0.05 V (max), VOH = 4.95 V (min) for VDD = 5V, VIL = 1.5V (max), and VIH = 3.5V (min).
Noise margin calculation:
NML = VIL – VOL = 1.5V – 0.05V = 1.45V
NMH = VOH – VIH = 4.95V – 3.5V = 1.45 V

Propagation Delay (tp) Calculation:
Tplh = 55 ns (typ.), 110 (Max.)
Tphl = 55 ns (typ.), 110 (Max.)
For typical values:
Tp = (tplh + tphl) / 2 = (55 ns + 55 ns) / 2 = 55 ns
For Max values: tp = 110 ns

Therefore, the noise margins and propagation delay calculated agree with the values by the CD4007 datasheet according to the values found from the experiment.

Conclusion

The VTC and propagation delay experiment demonstrated how understanding its behaviour, determining the switching threshold, and noise margin ensures the inverter's noise immunity and reliability. Propagation delay measures how the inverter switches its states and how it would impact the curves.

Experiment 2: 2-Ring oscillator

Introduction

In this experiment, a three-stage ring oscillator was constructed using the CD4007 chip, leveraging irs CMOS inverters. By connecting the outputs of the three inverters in a loop, the circuit produces continuous oscillations due to the inherent propagation delays on the CMOS transistors. This setup allowed for measuring the oscillator's frequency and relating ti to the propagation delay measured in the prior experiment. The ring oscillator demonstrates how timing characteristics in digital circuits can be exploited to create periodic signals, which are critical in clock generation and signal processing applications.

Observations

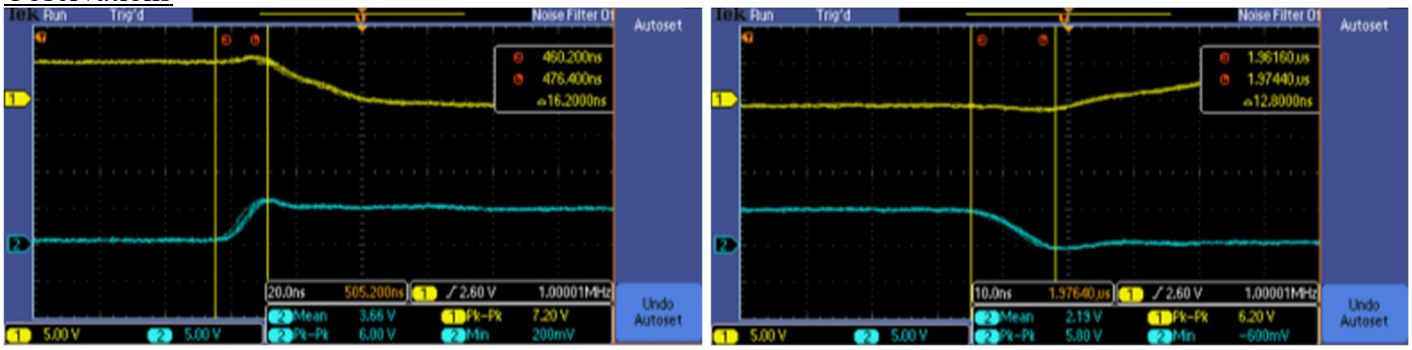


Figure 2: *The image on the left is v1 tplh, and the image on the right is v1 tphl.*

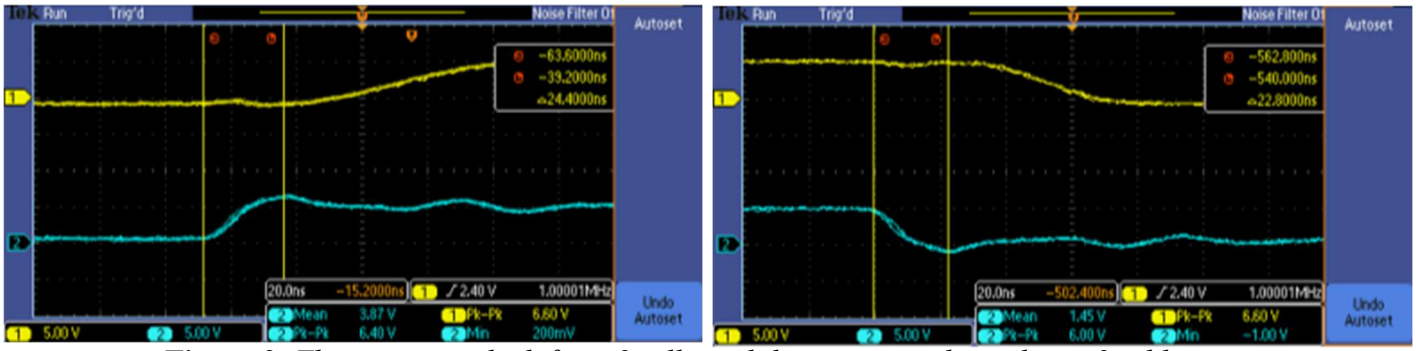


Figure 3: *The image on the left is v2 tplh, and the image on the right is v2 tphl.*

Analysis

Frequency of oscillation (f) for a ring oscillator, inverters are represented by (n), and propagation delay (tp) calculation:

f = 1/ (2ntp) = 1/ (2 *3 * 55) = 30.30 MHz

fmax = 1/ (2ntp) = 1/ (2 *3 * 110) = 15.15 MHz

The frequency can be adjusted by changing the number of inverters or modifying the propagation delay. It can also be adjusted by changing the supply voltage (VDD) or changing the load capacitance. The frequency relates to the propagation delay as when increasing the number of inverters increases the total propagation delay which results in a lower frequency oscillation. Lowering supply voltage increases the propagation delay of each inverter, which lowers the frequency and increasing the load increases propagation delay which decreases the frequency. All of these are true for if the opposite is done.

Conclusion

The ring oscillator experiment successfully demonstrated how propagation delay in CMOS inverters can be utilized to generate oscillatory signals. The frequency of the oscillator was observed and analyzed, showing its dependence on the inherent delays of the inverters. This experiment increased our understanding of the timing dynamics in CMOS circuits and highlighted their practical applications in oscillator design.

Experiment 3: NAND, NOR and NOT gates

Introduction

This experiment focused on understanding the behaviour of NAND and NOR gates using the CD4011 and CD4001 chips respectively. By analysing the Voltage Transfer Characteristics (VTC) of these gates and constructing their truth tables, the logical operations were verified. Additionally, LED logic level indicators were employed to observe the output states (high or low) in a digital format, providing a visual understanding of gate operations. Building on this concept the experiment explored the flexibility of logic gates, including constructing a NOT gate using a NAND gate and deriving a NOR gate from NAND gates. This study teaches us the foundational logic in digital circuit design and operation

Setup

1. Connect pin 14 of both chips CD4011 and CD4001 to 5V supply (V_{DD})
2. Connect pin 7 of both chips to ground (V_{SS})
3. Use the V_{SS} & V_{DD} to provide logical inputs to chips (1 = 5V and 0 = 0V)

4. Record the resultant voltages from the output using a voltmeter
5. Do the same experiment but replace the voltmeter with parallel LEDs using 1kΩ resistors in series and the cathode to ground for proper logic level indication
6. Record the observations of the LEDs at all logic settings
7. For the **NOT** gate (from CD4011 chip) connect both inputs of NAND gate together.
8. Verify the logic via observations.

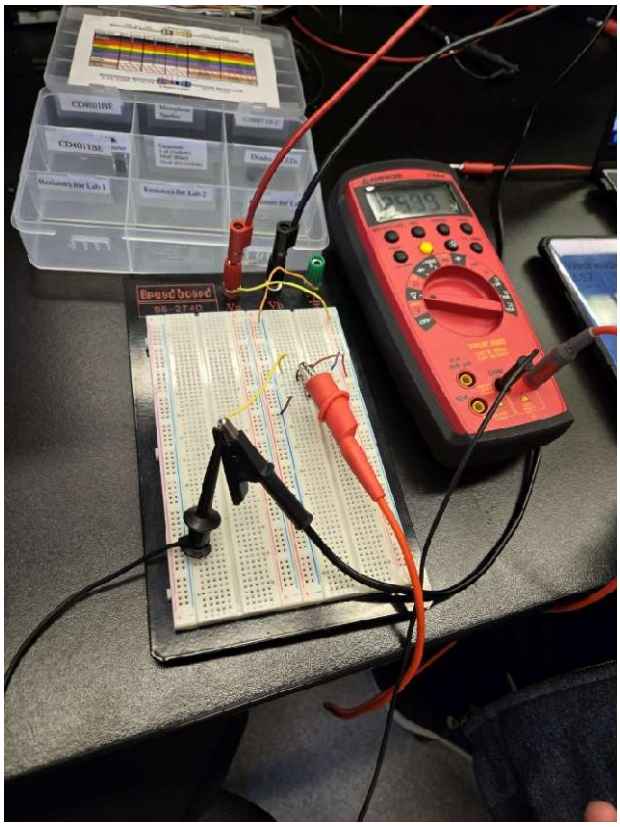
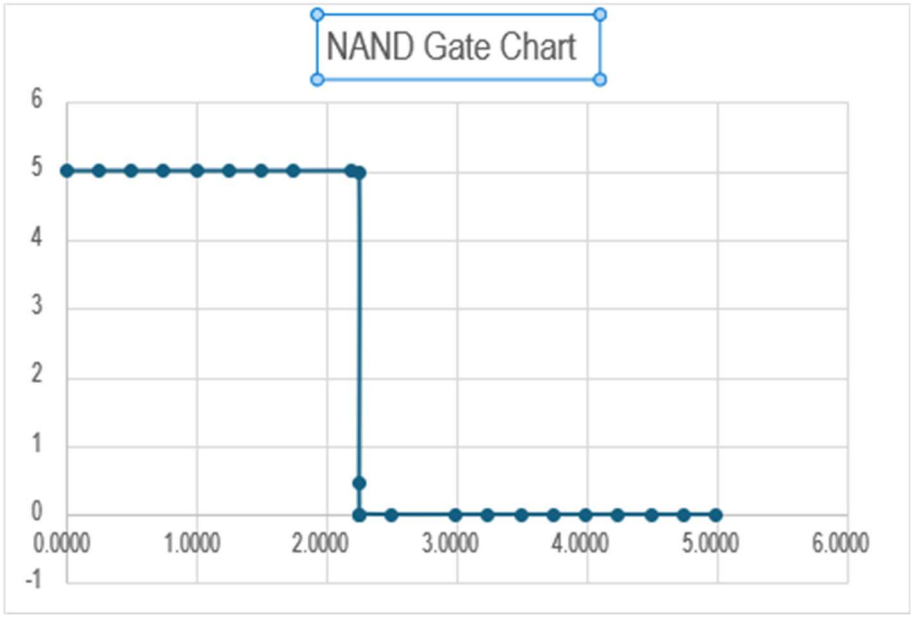


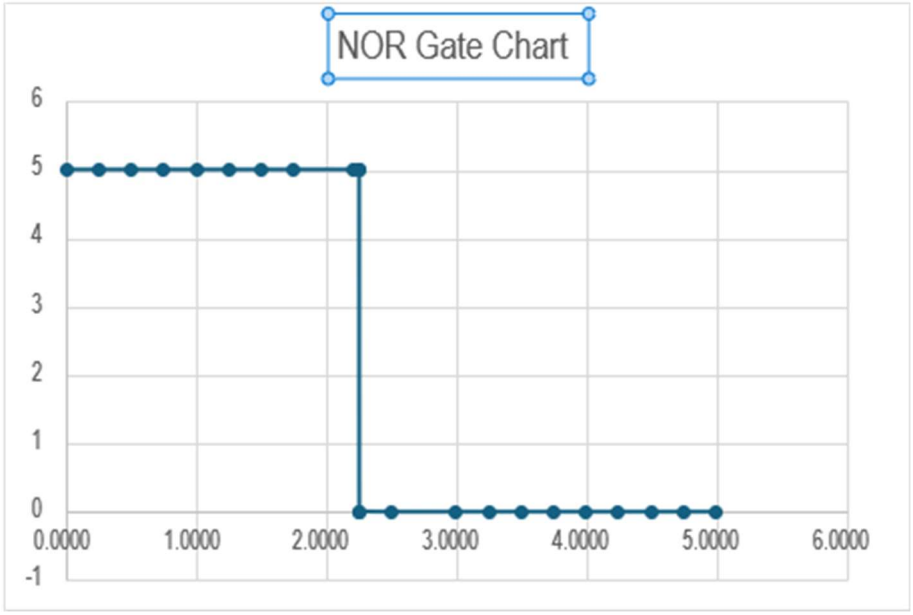
Figure 4: Experiment 3 Setup

Observations

		NAND					NOR	
A	B	Green LED	RED LED		A	B	GREEN LED	RED LED
0	0	1	0		0	0	1	1
0	1	0	1		0	1	0	1
1	0	0	1		1	0	0	1
1	1	0	1		1	1	0	1

Table 1: Table showing results of NAND & NOR Gate analysis using LEDs



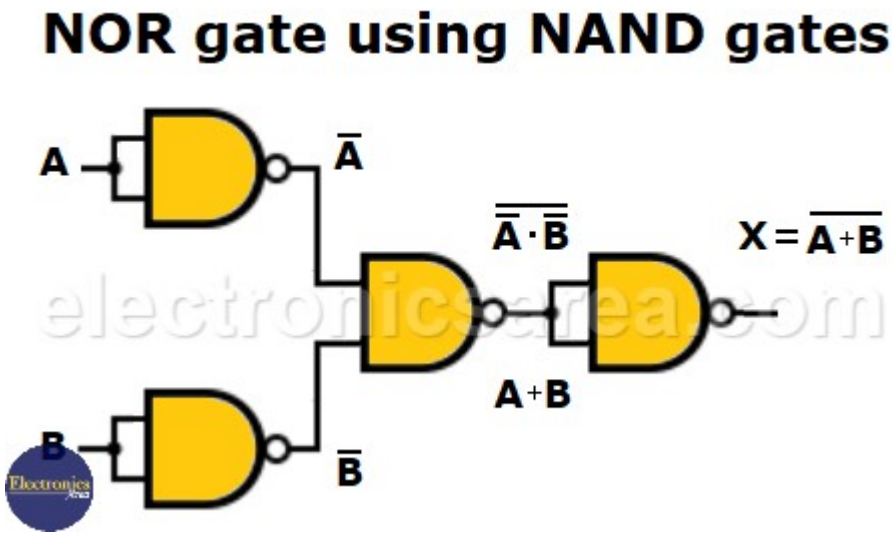


Analysis

As it can be seen from the observations above, the tables justify their respective names NAND and NOR. As we know from our theoretical knowledge the expected truth tables for both, using our pre-existing knowledge we can verify the expected outputs for these and indeed our outputs did math with the expectations.

A NAND gat can function as a NOT gate as is shown from our experiment. When the inputs of a NAND gate are connected together then the out put becomes a not of the inputs, for example if both inputs are 1 (high) then the output becomes 0 (low) and vice versa.

A NAND gate can also be used to create a NOR gate by using this identity $\overline{A + B} = \bar{A} \,.\, \bar{B}$. Since we already know that a NAND gate can be converted to a NOT we can use this to create a NOR gate using only NANDS.



Conclusion

The logic gates experiment provided valuable insight into the operations and versatility of digital logic gates. The use of LED logic level indicators provided an intuitive and visual way to verify output states, enhancing the understanding of digital logic operations. By characterizing the NAND and NOR gates and verifying their truth tables, the fundamental principles of digital logic were reinforced. The practical exercises in deriving the logic functions, such as creating a NOR gate from NAND gates highlighted the flexibility and utility of basic logic components in digital degisn, these activities deepen our understanding of logic circuits and their role in complex digital systems

References

[1] M. A. El-Nasr, and S. Gregori, *ENGG*3450 Electronic Devices- Laboratory #2 Manual Fall 2024.* (2024). University Of Guelph [Accessed: 11-Nov-2024]

[2] M. A. El-Nasr. *ENGG*3450 Electronic Devices- Lecture 14, 17-21 2024.* (2024). University Of Guelph [Accessed: 11-Nov-2024]